D. Remarks

Objections to Claims.

Claims 5, 9 and 12 have been amended to address the claim objections.

Rejection of Claims 9 and 10 Under 35 U.S.C. §103(a), based on U.S. Patent No. 5,300,798 (*Yamazaki et al.*) in view of U.S. Patent No. 5,733,816 (*Iyer et al.*).

The invention of claim 9 is directed to a semiconductor apparatus having a plurality of functional circuit blocks. Each functional circuit block includes a plurality of device elements, a first wiring region and a second wiring region. The semiconductor apparatus also includes a multi-layer wiring configuration containing a plurality of wiring layers. The multi-layer wiring configuration includes a first wiring layer disposed in the first wiring region providing first wiring in a first direction. Further, the first wiring layer is disposed in the second wiring region providing a second wiring in a second direction. The semiconductor apparatus further includes a predetermined first portion of the first wiring layer being electrically connected to and disposed in parallel with wiring in a second one of the plurality of wiring layers. The second wiring layer has a higher sheet resistance than the first wiring layer

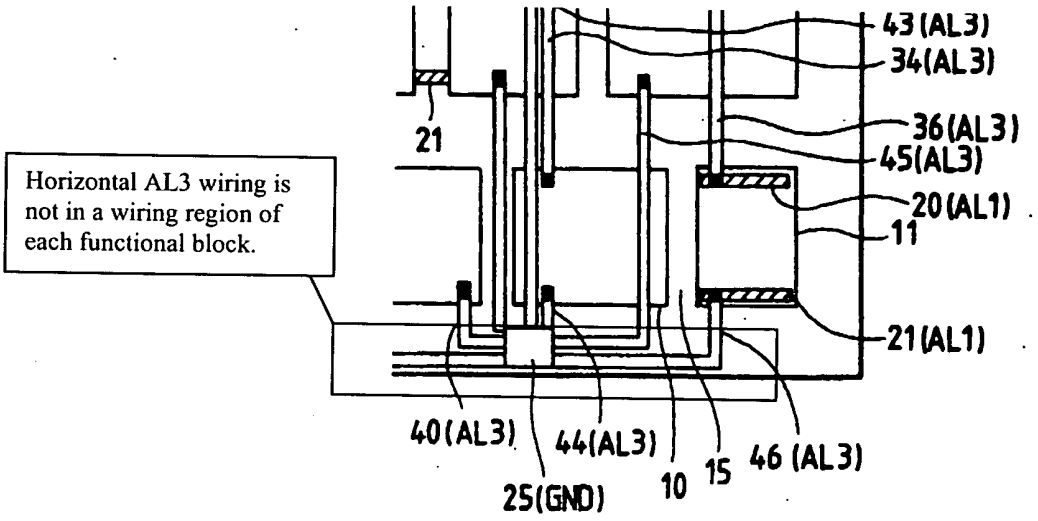
As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

As emphasized above, in Applicant's claim 9 invention, each functional circuit block includes both a first wiring region and a second wiring region. Still further, in the first wiring region the first wiring layer provides a first wiring in first direction. In the second wiring region, the second wiring layer provides a second wiring in a second direction. Such a limitation is not believed to be shown or suggested in the cited combination of references.

Yamazaki et al. shows a semiconductor integrated circuit device having a power supply wiring with multiple aluminum wirings AL1 to AL3 (argued to correspond to Applicant's "multilayer wiring"). Wiring layer AL3 of *Yamazaki et al.* has regions in which the wiring layer is provided in first and second directions.

As shown in the below portion of FIG. 3 of *Yamazaki et al.*, wiring AL3 includes

portions that extend in a first direction (horizontal) and a second direction (vertical). However, the horizontal portion cannot be considered to be in either a first or second wiring region, as the wiring is outside of the functional circuit blocks, and not included in each circuit block.



Accordingly, the cited reference *Yamazaki et al.* is not believed to show first wirings in first wiring regions and second wirings in second wiring regions, as recited in claim 9. Because *Yamazaki et al.* appears to maintain horizontal AL3 wirings outside regions of all functional blocks, the reference is not believed to be suggestive of such a limitation, either.

The remaining reference, *Iyers et al.*, is directed to depositing a tungsten layer, and hence provides no further teachings regarding a "multi-layer wiring configuration containing a plurality of wiring layers", as recited in claim 9.

Because the combination of references does not or suggest all limitations of claim 9, this ground for rejection is believed to be traversed.

Claims 5, 9 and 12 have been amended, not in response to the cited art, but to address claim objections. The present claims 3-6, 9-10 and 12 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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